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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/063,883	05/21/2002	Chien-Fa Wang	VIAP0033USA	2356

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NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE)
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EXAMINER	
TRUONG, BAO Q	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/063,883	WANG, CHIEN-FA	
	Examiner	Art Unit	
	Bao Q Truong	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,12-17,25 and 26* is/are rejected.

7)☒ Claim(s) *5-11 and 18-24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☒ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The instant application having Application No. 10/063,883 has a total of 26 claims pending in the application; there are 2 independent claims and 24 dependent claims, all of which are ready for examination by the examiner.

Oath/Declaration

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. § 1.63.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan on 4 October 2001. Furthermore, it is noted that applicant has filed a certified copy of the 090124574 application as required by 35 U.S.C. 119(b).

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

Specification

5. The disclosure is objected to because of the following informalities:

Abstract of disclosure recites "Amethod for data accessing" on line 1, "the basic input/outputsystem" on line 4, "memorywhen" on lines 5 and 8.

Summary of invention recite "memorywhen" on lines 6 and 9.

Appropriate correction is required.

Claim Objections

6. Claims 1 and 14 are objected to because of the following informalities:

Claim 1 recites "the basic input/outputsystem" on lines 3-4, "inthe" on line 6, "memorywhen" on lines 7 and 12, "updatedata" on line 9.

Claim 14 recites "the basic input/outputsystem" on line 3, "inthe" on line 7, "memorywhen" on lines 8 and 12.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-4, 12-17, and 25-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Piwonka et al. (U.S. Patent No. 6,073,206).

Referring to claim 1, Piwonka teaches a method for accessing data in a computer, the computer comprising a non-volatile memory and a volatile memory (see figure 1: elements 20 and 78), the non-volatile memory comprising a first portion and a second portion, the first portion storing the basic input/output system (BIOS) of the computer (see column 4: lines 61-65), the method comprising:

allocating data in the second portion of the non-volatile memory to the volatile memory when the computer starts up as following boot-up of the computer system, initiating Power-On-Self-Test (POST), copying a ROM image of the Extended System Configuration Data (ESCD) from an ESCD sector to an ESCD original buffer and an ESCD write buffer (see figure 3, figure 4: steps 200-202, column 2: lines 39-51, column 5: lines 50-67, and column 6: lines 55-60);

updating corresponding data stored in the volatile memory when a user wants to update data stored in the second portion of the non-volatile memory as copying the contents of the

ESCD write buffer to an ESCD runtime buffer during POST (see figure 3, figure 4: step 204, column 2: lines 51-55, and column 6: lines 55-60), if a write is performed to ESCD data or an associate variable during runtime, updating the ESCD runtime buffer with ESCD data or variable provided for the write operation (see figure 4: steps 212-214 and column 6: lines 27-39); and

writing back the data in the volatile memory to the second portion of the non-volatile memory as flashing the new ROM image in the ESCD runtime buffer into the ESCD sector during a system management mode of the computer system (see column 6: lines 39-46).

Piwonka further teaches that ESCD is updated during runtime by system software in order to effect configuration of devices **on the next boot** (see column 1: lines 66-67 and column 2: line 1). However, Piwonka does not clearly teach writing back the data in the volatile memory to the second portion of the non-volatile memory **when the computer is ready to shut down**.

The examiner takes "Official Notice" that it would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the method taught by Piwonka so the step of writing back the data in the volatile memory to the second portion of the non-volatile memory occurs **when the computer is ready to shut down**. This would have been obvious because of the following reasons. First, more modifications can be made as deemed necessary; by postponing the writing back step until the computer is ready to shut down, only the most up-to-date data is flashed back to the non-volatile memory. Furthermore, by postponing the writing back step until the computer is ready to shut down, access delay can be avoided. This is similar to changing system configuration in Windows™: modifications are hold in registers and flashed into BIOS when the computer is shut down and configuration will be effected on the next boot.

As to claim 2, Piwonka further teaches, when the user wants to update the data stored in the second portion of the non-volatile memory, a corresponding update operation is executed in the volatile memory without modifying the data in the second portion of the non-volatile memory as an image of the ESCD sector is stored in the ESCD runtime buffer during POST (see figure 3, figure 4: step 204, column 2: lines 51-55, and column 6: lines 55-60), if a write is performed to ESCD data or an associate variable during runtime, the ESCD runtime buffer is updated with ESCD data or variable provided for the write operation (see figure 4: steps 212-214 and column 6: lines 27-39).

As to claim 3, Piwonka further teaches that the non-volatile memory includes BIOS code, additional code, and ESCD (see column 4: lines 61-67 and column 5: lines 1-4). The non-volatile memory inherently comprises a plurality of blocks as basic storage units for storing data. The examiner has also provided a copy of Extended System Configuration Data Specification for the applicant's convenience of understanding the examiner's position.

As to claim 4, Piwonka further teaches that the volatile memory comprises a plurality of sectors corresponding to the blocks of the second portion of the non-volatile memory as ESCD original buffer, ESCD write buffer, and ESCD runtime buffer are random access memory areas (see figure3: element 108-112 and column 6: lines 55-60); and the data stored in the blocks of the second portion of the non-volatile memory are allocated to the corresponding sectors of the volatile memory when the computer starts up as following boot-up of the computer system,

initiating POST, copying a ROM image of the ESCD from an ESCD sector to an ESCD original buffer and an ESCD write buffer (see figure 3, figure 4: steps 200-202, column 2: lines 39-51, column 5: lines 50-67, and column 6: lines 55-60).

As to claim 12, Piwonka teaches the method of claim 1 in a computer environment. However, Piwonka does not clearly teach that the computer is an information appliance.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to use the method taught by Piwonka in an information appliance. This would have been obvious because the information appliance has a basic structure of a computer. However, the amount of system resource, especially RAM, is very limited for the information appliance. Furthermore, RAM is often used up to store data while ROM is normally used to store only BIOS. The method of Piwonka allows updating data stored in a non-volatile memory at a reduced execution time. So, a portion of data can be stored in ROM besides RAM. Therefore, the system resource is efficiently used.

As to claim 13, Piwonka further teaches that the non-volatile memory is a flash memory and the volatile memory is a random access memory (see column 2: lines 39-55, column 4: lines 61-65, and column 6: lines 55-60).

Referring to claim 14, Piwonka discloses a computer comprising:

a non-volatile memory comprising a first portion for storing the basic input/output system (BIOS) of the computer and a second portion (see figure 1: element 78 and column 4: lines 61-65);

a volatile memory for storing data temporarily during operation of the computer (see figure 1: element 20); and

a processor (see figure 1: element 32); wherein

the processor allocates data stored in the second portion of the non-volatile memory to the volatile memory when a user starts up the computer as following boot-up of the computer system, initiating Power-On-Self-Test (POST), copying a ROM image of the Extended System Configuration Data (ESCD) from an ESCD sector to an ESCD original buffer and an ESCD write buffer (see figure 3, figure 4: steps 200-202, column 2: lines 39-51, column 5: lines 50-67, and column 6: lines 55-60);

the processor updates data stored in the volatile memory when the user wants to update corresponding data stored in the second portion of the non-volatile memory copying the contents of the ESCD write buffer to an ESCD runtime buffer during POST (see figure 3, figure 4: step 204, column 2: lines 51-55, and column 6: lines 55-60), if a write is performed to ESCD data or an associate variable during runtime, updating the ESCD runtime buffer with ESCD data or variable provided for the write operation (see figure 4: steps 212-214 and column 6: lines 27-39); and

the processor writes back the updated data in the volatile memory to the non-volatile memory as flashing the new ROM image in the ESCD runtime buffer into the ESCD sector during a system management mode of the computer system (see column 6: lines 39-46).

Piwonka further discloses that ESCD is updated during runtime by system software in order to effect configuration of devices **on the next boot** (see column 1: lines 66-67 and column 2: line 1). However, Piwonka does not clearly disclose the processor writes back the updated data in the volatile memory to the non-volatile memory **when the user is ready to shut down the computer**.

The examiner takes "Official Notice" that it would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to modify the computer disclosed by Piwonka so the processor writes back the updated data in the volatile memory to the non-volatile memory **when the user is ready to shut down the computer**. This would have been obvious because of the following reasons. First, more modifications can be made as deemed necessary; by postponing the writing back step until the computer is ready to shut down, only the most up-to-date data is flashed back to the non-volatile memory. Furthermore, by postponing the writing back step until the computer is ready to shut down, access delay can be avoided. This is similar to changing system configuration in Windows™: modifications are hold in registers and flashed into BIOS when the computer is shut down and configuration will be effected on the next boot.

As to claim 15, Piwonka further discloses, when the user wants to update the data stored in the second portion of the non-volatile memory, a corresponding update operation is executed in the volatile memory without modifying the data in the second portion of the non-volatile memory as an image of the ESCD sector is stored in the ESCD runtime buffer during POST (see figure 3, figure 4: step 204, column 2: lines 51-55, and column 6: lines 55-60), if a write is performed to ESCD data or an associate variable during runtime, the ESCD runtime buffer is updated with ESCD data or variable provided for the write operation (see figure 4: steps 212-214 and column 6: lines 27-39).

As to claim 16, Piwonka further discloses that the non-volatile memory includes BIOS code, additional code, and ESCD (see column 4: lines 61-67 and column 5: lines 1-4). The non-volatile memory inherently comprises a plurality of blocks as basic storage units for storing data. The examiner has also provided a copy of Extended System Configuration Data Specification for the applicant's convenience of understanding the examiner's position.

As to claim 17, Piwonka further discloses that the volatile memory comprises a plurality of sectors corresponding to the blocks of the second portion of the non-volatile memory as ESCD original buffer, ESCD write buffer, and ESCD runtime buffer are random access memory areas (see figure3: element 108-112 and column 6: lines 55-60); and the data stored in the blocks of the second portion of the non-volatile memory are allocated to the corresponding sectors of the volatile memory when the user starts up the computer as following boot-up of the computer system, initiating POST, copying a ROM image of the ESCD from an ESCD sector to an ESCD

original buffer and an ESCD write buffer (see figure 3, figure 4: steps 200-202, column 2: lines 39-51, column 5: lines 50-67, and column 6: lines 55-60).

As to claim 25, Piwonka teaches the computer of claim 14. However, Piwonka does not clearly teach that the computer is an information appliance.

It would have been obvious to one having an ordinary level of skill in the art at the time the invention was made to use the computer structure disclosed by Piwonka in an information appliance. This would have been obvious because the information appliance has a basic structure of a computer. However, the amount of system resource, especially RAM, is very limited for the information appliance. Furthermore, RAM is often used up to store data while ROM is normally used to store only BIOS. The method of Piwonka allows updating data stored in a non-volatile memory at a reduced execution time. So, a portion of data can be stored in ROM besides RAM. Therefore, the system resource is efficiently used.

As to claim 26, Piwonka further discloses that the non-volatile memory is a flash memory and the volatile memory is a random access memory (see column 2: lines 39-55, column 4: lines 61-65, and column 6: lines 55-60).

Allowable Subject Matter

9. Claims 5-11 and 18-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Form PTO-892.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bao Q Truong whose telephone number is (703) 308-7090. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A Sparks, can be reached on (703) 308-1756. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

BAO QUOC TRUONG
BT
Patent Examiner
2 March 2004

Donald Sparks
Supervisory Patent Examiner
Technology Center 2100